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Fast Capacitance-to-Digital Converter with Internal Reference

Kaiyuan Gao, Delong Shang, Fei Xia and Alex Yakovlev
Low Power Embedded System Design Laboratory, uSystems Group, School of EEE
Newcastle University
Newcastle upon Tyne, NE1 7RU, UK
{*k.gao,delong.shang,fei.xia,alex.yakovlev*}@ncl.ac.uk

***Abstract*—Conventional capacitance-to-digital converters (CDC) widely used in IoTs particularly in portable applications tend to make use of complex analog-to-digital technologies. However this can be power hungry and take long conversion time. In addition, the analog parts are hard to implement in ASICs, especially under wide working conditions, such as energy harvesting scenarios. Recently digitalized CDCs were proposed to meet these challenges, but existing solutions still required long conversion time, and need external voltage references limiting their portability. A novel CDC with low energy consumption and short measuring time is presented in this paper. With a new internal time reference method, it is fully portable and achieves fast conversion response. A method of decoupling the sensing resolution from the discharge mechanism enhances the programmability of such sensors making energy to precision tradeoffs straightforward. This paper contains both theoretical analysis and the experimental demonstration of these methods. This new solution can reduce the conversion time by more than 20 times, and reduce energy consumption by half.**

Keywords—internal time references; start-stop mechanism; capacitance-to-digital; counting; low power; conversion time; voltage controlled oscillator.

I. INTRODUCTION

New application areas, such as wearable devices, environmental monitoring, smart buildings, and especially medical applications including patient monitoring and bio-implants have been emerging as application areas for embedded systems [1][2]. Capacitance-to-digital converters (CDCs) play a very important role in such applications [4]. The application cases often need small device and battery sizes [3]. Capacitive sensors with low energy consumption and no static power therefore have an advantage [4].

The conventional approach to CDC consists of a capacitance-to-voltage converter (CVC) and an analog-to-digital converter (ADC) [5][6]. The measured capacitance is converted to voltage by the CVC, and the ADC is used to convert the voltage to digital code [3][7]. In order to improve the resolution, switched-capacitor $\Delta\sum$ converters have been used which also need ADC [8]. This complexity and need for analog components tend to lead to higher energy consumption, lower accuracy robustness and larger chip area [9][10].

In addition to lower energy consumption, conversion response time is also an important metric for CDCs. As a possible solution, a full digital CDC was presented in [10]. It includes a sensed capacitor (C_{sense}), an inverter ring oscillator (or equivalent mechanism), and an event recording component, avoiding analog circuits. This digitalized CDC measures C_{sense} through monitoring its discharge process.

The solution in [10] has several problems. [12] proposed a new solution which solves these problems. Both make use of an explicit voltage reference, V_{low}. C_{sense} has to discharge from an initial voltage to V_{low}. Normally V_{low} is quite low, as a result, this discharge requires a substantial amount of time to finish. In addition, although power figures are lower compared to conventional CDCs, they remain high in an absolute sense.

In this paper we propose and implement a novel CDC based on a time comparator (TC), aiming at shortening the conversion time and lowering the energy consumption. A voltage controlled oscillator (VCO) is powered by the charge on C_{sense}, which is initially charged to a known voltage V_{dd}. The number of VCO cycles when the capacitor is discharged is almost linear to the value of the sensed capacitors under any particular V_{dd} [10][12]. It means that the value of C_{sense} can be derived by measuring the discharge time.

The main contributions of this paper include the theoretical foundations of the proposed method and a novel CDC design based on this method, which includes a new method to detect the frequency, a method to end the discharge without needing a reference voltage, and a method of decoupling the sensing precision from the decision on when to end the discharge.

The remainder of this paper is organized as follows. In Section II, the proposed CDC is described, including the theory of digital conversion. Section III presents the implementation of the proposed TC. Section IV gives the experimental results in UMC 90nm CMOS technology. Finally, this paper is concluded in Section V.

II. ANALYSIS AND THEORY OF THE PROPOSED CDCS

The theory of the digitalized CDC can be partially found in [10][12]. The value of a sensed capacitor (C_{sense}) is converted to digital codes through recording its discharge process.

A. Capacitance to Time Converter

The digitalized CDC methods firstly convert capacitance to time using the mechanism as shown in Fig. 1. Firstly C_{sense} is charged to a known voltage, V_{dd}, then the two switches are operated so as to disconnect C_{sense} from V_{dd} and discharge it through the load, i.e. the digital conversion block (DCB).

Pragmatically, instead of discharging to 0V, which theoretically takes an infinite amount of time regardless of the value of C_{sense}, we discharge to some pre-set constant $V_{low} > 0$, at which point the discharging is stopped and the time value

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recorded. In this case, the length of time the discharge process takes is determined by the value of C_{sense}, and the mechanism can be used to convert capacitance to time.

We assume that V_{low} is a design specification, and the system must be able to support any known choice of V_{low}, which must satisfy $V_{dd} > V_{low} > 0$.

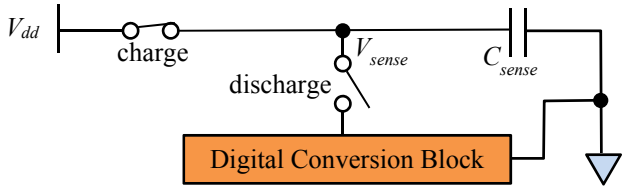

Fig. 1. Digital CDC architecture.

B. Capacitor discharge process

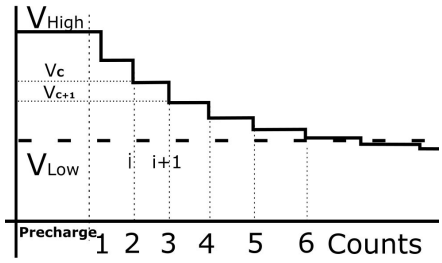

Fig. 2. Discharge process.

The iterative delay chain discharge method used in [10][12] is based on the following theory [12][13]. Fig. 2 shows the capacitance to digital discharge process. At step i, Q_i will be $C_{sense} * V_i$, and at step i+1, Q_{i+1} will be $C_{sense} * V_{i+1} + C_p * V_{i+1}$ where C_p is the parasitic capacitors of the inverter chain. As $Q_i = Q_{i+1}$, so $C_{sense} * V_i = (C_{sense}+C_p) * V_{i+1}$, the following formula is derived:

$$\frac{V_{i+1}}{V_i} = \frac{C_{sense}}{C_{sense}+C_p} \quad (1)$$

and as $V_{i+1} = V_i(1-k)$, then $k = \frac{C_p}{C_{sense}+C_p}$ (2)

And then the discharge process is modelled by using the equation: $V_{low} = V_{high}(1-k)^n$ (3)

where n is the number of steps taken to discharge V_{sense} from V_{high} to V_{low}, and can be used to represent V_{high}. And based on Taylor's series, the formula $(1-k)^n$ can be represented as:

$$1 - nk + {}^{n*(n-1)k^2}/_{2*1} - {}^{n*(n-1)*(n-2)k^3}/_{3*2*1} + \cdots$$

If $nk << 1$, the above formula can be shortened as:

$$1 - nk \quad (4)$$

From (3), if V_{high} and V_{low} are fixed (i.e. const.) by the measurement method, then we must have $(1-k)^n = const$. Thus, under $nk << 1$, we have $1 - nk = const$ and thus $nk = const$, and hence $n\frac{C_p}{C_{sense}+C_p} = const$, so if $C_{sense} + C_p \approx C_{sense}$, we will have $\frac{nC_p}{C_{sense}} = const$, and thus n must be linearly proportional to C_{sense}.

C. Proposed high frequency clock generator

The key of the digitalized CDCs is therefore accumulating a number which corresponds to cycles of oscillation during the discharge process. If the period of a cycle is T_{cycle}, then

$$\#\ of\ cycles = \frac{t}{T_{cycle}} \quad (5)$$

Some existing solutions, e.g. [10][12] use a constant oscillation frequency, which corresponds to the frequency of the DCB operating under V_{low}, the lower voltage bound of the V_{sense} discharge process. This makes sense in that this frequency is possible to maintain across the entire discharge process and also usually low enough to provide good power figures.

Inverter ring oscillators can be used as a clock generator, and also as the discharge circuit in a CDC. This leads to cycles not directly measuring t but linear with C_{sense}. As the oscillator is powered by C_{sense} which is pre-charged to $V_{sense} = V_{dd}$, during discharge, the oscillator's frequency is related to V_{sense} which reduces as C_{sense} discharges. The frequency changes with time, to maintain linearity between the count and C_{sense}.

The relationship between V_{sense} and the oscillator frequency F is expressed as:

$$F = \alpha V_{sense} + b \quad (6)$$

Where α is a constant measured in Hz/V; b is the offset, also a constant, in Hz. During the discharge, F reduces and T_{cycle} increases with the reduction of V_{sense}.

If the discharging process is stopped when V_{sense} reduces to some lower bound V_{low}, we have the following:

$$T_{cycle}(V_{sense}) \leq T_{cycle}(V_{low}) \quad (7)$$

This means that the cumulative precision is higher than the lower bound determined by V_{low}.

D. Internal Reference – Time Reference for V_{low}

To end the discharging process, [10][12] use an explicit V_{low}, which is assumed to come from some external reference source, hence sidestepping the usual difficulties associated with generating a high quality voltage reference. In addition, the energy charged into C_{sense} is discharged to V_{low}, and the external V_{low} is used to power a circuit to generate $T_{cycle}(V_{low})$. This consumes extra energy.

This paper uses a new method for internally achieving the same function as a specified V_{low}, i.e. stopping the discharge at the right point, without depending on an external reference. Internalizing the reference leads to more complete and stand-alone solutions with much wider applicability and better portability. And the energy in C_{sense} is all that is used for the entire conversion. As F is a function of V_{sense}, stopping discharging at a pre-set V_{low} is the same as stopping discharging at a pre-set $F_{low} = F(V_{low})$, the frequency at V_{low}.

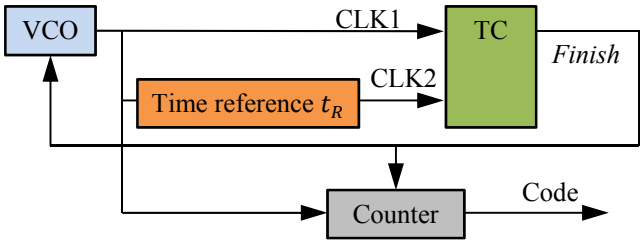

Fig. 3. Block diagram of the proposed CDC.

The mechanism originally proposed in [11] for detecting voltage changes can then be used here to detect, removing any external references, whether any particular F_{low} has been

reached, as it detects whether the time distance between two consecutive cycles has reached a certain value:

$$T_{cycle} = 1/F_{low} \quad (8)$$

In other words, the distance between two consecutive cycles (the signal's period) increases as the voltage reduces. When it becomes equal to $1/F_{low}$, the discharge process is stopped and the time taken to calculate C_{sense}.

E. Summary

This leads to a solution where the oscillation signal, generated by a voltage controlled oscillator (VCO) only needs to be compared with a delayed version of itself. The oscillation signal is also used to trigger a counter to count the number of clock cycles as shown in Fig. 3. The discharge stops when the distance between two clock cycles increases to a pre-set delay (time reference) value t_R, with $t_R = 1/F_{low}$. In addition to the VCO and counter, the scheme uses a delay (with a value of t_R) and a time comparator (TC).

III. Implementation

A. Time reference

The CDC draws its power from the variable V_{sense}, an internal time reference is therefore easier to implement than an internal voltage reference. In this CDC, the delay is implemented with an RC circuit whose latency is independent of the working voltage. The scheme is shown in Fig. 4.

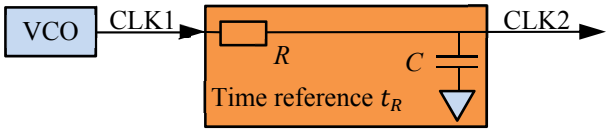

Fig. 4 Two consecutive clocks with time reference.

The values of R and C can be tuned so that $t_R = 1/F_{low}$.

B. Time comparator

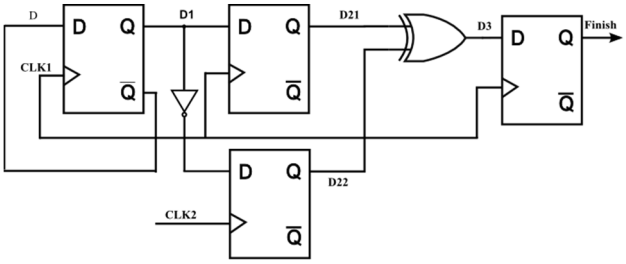

Fig. 5. TC – time comparator.

Fig. 5 shows the time comparator (TC), which includes four D flip-flops (DFFs), one inverter and one XOR gate. It is based on the 'shadow register' idea [11].

CLK2 is CLK1 delayed by the time reference t_R, set to $T_{cycle}(V_{low})$. The voltage starts from V_{dd} and discharges down towards V_{low} monotonically. When the frequency of these CLK signals (F) is higher than $1/t_R$, indicating $V_{sense} > V_{low}$, D22 is set to not D21 sometime after D21 has arrived at the XOR gate, which sees D22=D21 and outputs 0. *Finish* is latched to false, allowing the discharging process to continue for one more cycle. When F eventually reduces to $F \approx 1/t_R$, D21!=D22 arrive close together at the XOR gate and $Finish = true$ to end discharging. This is because D21 represents CLK1 delayed by one CLK cycle $T_{cycle} = 1/F$ and D22 represents CLK1 delayed by t_R and the event being detected by the TC is $T_{cycle} = t_R$, which means $V_{sense} = V_{low}$.

This is a completely novel use of this TC design, which was originally used in [11] to detect when two CLK signals achieve the same frequency. Fig. 6 is obtained from an example simulation run, demonstrating the scheme, with the Finish signal becoming true when and only when $T_{cycle} = t_R$.

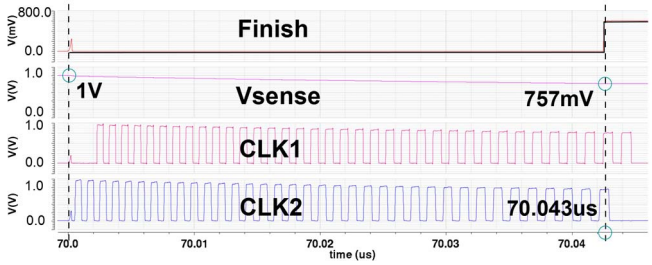

Fig. 6. Waveforms of simulation results.

IV. Experimental Results

The proposed CDC is designed in UMC 90 nm CMOS technology using Cadence toolkits, and simulated under the Spectre analog simulation tools. To characterize the designs, the following experiments are explored with supply voltages at 0.9v, 1v and 1.2v, respectively, and the sensed capacitance range is arranged from 11.3 pF to 100 pF. In addition to the TC, a 16 bit counter is implemented to record the number of VCO oscillation cycles between $V_{sense} = V_{dd}$ and $V_{sense} = V_{low}$.

Fig. 7 shows the relationship of the output of the counter (code), power and energy with the value of the sensed capacitors. Here a low F_{low} is used to achieve V_{low} around 0.44V. From Fig. 7, we conclude that the relationship between energy, codes and value of the sensed capacitor is linear. And the power figure will be stable when the sensed capacitors is large ($C_{sense} \gg C_p$). This means that the code and energy increase with increasing value of C_{sense}. This also means that the power consumption does not change too much and the increase of energy is due to the increase of conversion time.

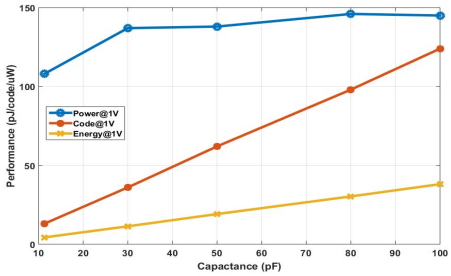

Fig. 7. Relationship of the codes, power, energy with different values of capacitors.

Further experiments cover different values of t_R, C_{sense} and V_{dd}. Fig. 8 shows the results with the relationship between time reference (t_R), sensed capacitance (C_{sense}) and output code in different discharge start voltages (V_{dd}).

For any C_{sense} s, the code is increased (higher sensing precision) with larger t_R (lower V_{low} to extend the discharge range). This is the tradeoff between sensing response time and precision. This demonstrates the method working in exactly the same way with multiple different V_{dd} values for wide applicability. For the same t_R value, the sensor has higher

precision under higher V_{dd} (higher system power). In other words, the precision of this sensor can be increased by either increasing the t_R value, likely a design-time decision, or increasing V_{dd}, which can be a run-time decision, both costing more energy and response time.

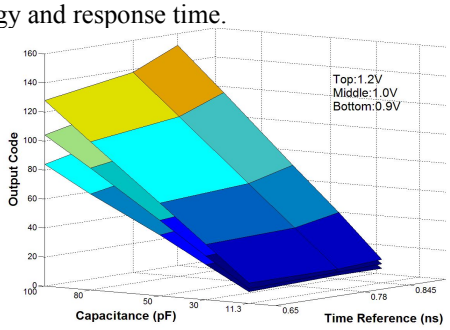

Fig. 8. Relationship under different V_{dd}s and different t_Rs.

The precision of the sensor is determined by the oscillation frequency in the VCO in this solution. However, there is no absolute need to use the VCO to trigger the counter directly and the functions of generating the *Finish* signal and generating the counting events can be fulfilled by different circuits, which would allow the further increase of sensing precision without trading sensing response time. This can be done by adding an extra fast oscillator to trigger the counter to record the clock cycles to decouple counter events from the *Finish* signal. This is shown in Fig. 9.

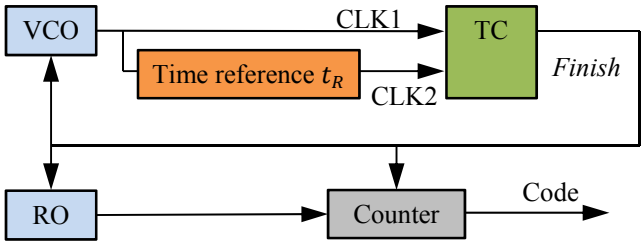

Fig. 9. Enhanced solution.

Table 1. Comparison Results (existing solutions)

	[4] JSSC 12	[3] ASSCC07	[10] ISSCC 15	[12] DDECS 16
Tecnology.	0.35µm	0.18µm	40nm	90nm
Method	Period Modulation	SAR ADC	Iterative Delay-Chain	Iterative Delay-Chain
Power	211µW	240µW	1.84µW	19.6µW
Meas. Time	7.6ms	4µs	19.06µs	0.95µs
Energy	1.161µJ	N/R	35.1pJ	19.3pJ
FoM (fJ/c-s)	139000	7937	141	N/R

$C_{sense} = 11.3pF$

Table 2. Comparison Results (this work)

	This work	This work (enhanced)
Technology	90nm	90nm
Method	Time Comparison	Time Comparison
Power	108µW	297µW
Meas. Time	0.04µs	0.036µs
Energy	4.33pJ	10.68pJ
FoM (fJ/c-s)	408	152

RO is started at the same time as VCO and the counter counts RO cycles. VCO and TC generate the *Finish* signal and VCO and RO all stop on *Finish*. The response time is tuned by V_{dd} and t_R as before, but precision is additionally improved by a factor λ: how much faster RO is than VCO.

The proposed CDC, the enhanced CDC, and several existing CDCs are all implemented using the same standard library and compared by using the same experiment data, where C_{sense}=11.3pF, discharged V_{dd} range from 1V down to 0.44V. Table 1 shows the performance of existing CDCs and Table 2 is the performance of this work. In this example we achieved 20X response time and 50% energy improvements.

V. Conclusions and Future Work

This paper presents a novel capacitance to digital convertor which is implemented based on the entirely novel idea of an internal time reference and a new way of using time comparators under Cadence tool kits. This is also a full digital solution without analogue components.

The internalization of the reference leads to enhanced portability and the change of reference from the voltage domain to the time and frequency domain reduces implementation cost, improves system robustness, and reducing the energy consumptions.

A method of generating faster counting events decouples the counting events from the end of sensing signal. This allows the sensing precision to be tuned independently from sensing response time and sensing energy to some extent.

The resulting design is demonstrated to improve both sensing response time and sensing energy when compared with a large number of existing designs in fair comparisons. The measuring response is 20 times faster and only half of the energy is consumed compared with the best existing cases.

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